



Date : 4/19/07

Job Description - Digital Chip Design Lead

A leading position in the IC design team in Canesta. Hands-on position, requiring direct involvement in the design work, development of processes, driving external contractors and leadership of digital design function.

Minimum Requirements

- BSEE or Equivalent, MSEE preferred.
- 4 years experience in custom digital IC design using Verilog RTL
- Experience in each of the following stages in product development
 - Chip block architecture and block specification for design implementation
 - Design of finite state machines, data and control interface blocks
 - Chip level & block level verification planning and implementation
 - Chip level & block level test coverage planning & test insertion. Specifying and verifying ATPG generation. Supporting verification of test patterns in simulation and on the ATE
 - Design synthesis, defining and meeting timing constraints through the physical design implementation flow
 - Interface with and driving the physical design implementation team

Additional Desired Experience

- Working knowledge of VHDL RTL
- Chip design validation at board / lab. level
- Image sensor control logic design
- Datapath implementation, design of custom data processing blocks for chip integration
- Integration of CPU IP into a chip architecture
- Logic design, synthesis, verification & validation for FPGA



Location

- Applicant will be an employee of Canesta but reside in India.
- Applicant is expected to travel to the US about 4 times a year for about 10 days each time.
- Applicant may work from home or from an office location in India.
- Applicant must be self-motivated, able to work by himself and interface directly to the company's main office.

Send resume to:

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